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EC 'GREEN PAPER' ON JESSI PROGRAM

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[Text of the "Green Paper" from the JESSI [Joint European Submicron Silicon] project planning committee of the EC]

CONTENTS

PREAMBLE

RECOMMENDATION OF THE JESSI PLANNING COUNCIL

"intelligent components"

By the end of this century chips will be involved in virtually all industrial processes and products and they will affect most aspects of human life. In some respects the introduction of chips can be compared to that of electricity. Before electricity was widely introduced, however, it remained for 50 years a plaything of the scientists. The Planning Council of the JESSI-project expects the development of chips to proceed much faster than that of electricity since chips had a much shorter incubation time.

Chips is the name given to ICs, the acronym for "Integrated-electrical-Circuits". It would perhaps be more appropriate to say that IC stands for Intelligent Component. The IC is the intelligent part of a product or process. It steers, regulates, senses, judges, calculates, amplifies, counts etc. It does so in a cheaper, faster and more reliable way than any other known device. ICs have spread at unparalleled speed through man-made items. It is clear that products and processes with intelligent components will ultimately replace most if not all current counterparts, and will at the same time enable "homo faber" to create new products and processes or manufacture products more cheaply or economically. The group, company or nation that can introduce this technology first will have a tremendous advantage over competitors, if the latter continue to use traditional methods. The "traditionalists" will be left behind and they will be faced with an unpleasant position comparable to that of the less developed countries today. This is why the production and application of ICs is of major strategic importance. If Europe is to function as a political and economic entity it cannot afford to rely on the USA and Japan for its technology. This does not mean that Europe should aim at complete self-sufficiency. But at least it must bring the 'balance of the chips trade' in equilibrium.

The JESSI-programme is designed to secure Europe's industrial and economic future. The programme is unique since it addresses the total industrial chain. It is vital that European

industry does not confine itself to making chips for existing systems; it must also be able to create and design new systems that make use of Intelligent Components. The JESSI-programme as described in this Green Book and the appendices is the result of the cooperation of a broad range of industries and research institutes during a one-year planning phase (1988). The programme consists of four sub-programmes: Technology, Equipment and Materials, Application, and Basic and Long-Term Research. It is recognized that certain parts of the JESSI-programme have fruitful relations with initiatives of the EC and of national governments in the stimulation of modern microelectronics.

The sub-programme Application is to be carried out jointly by the users and the IC-manufacturers. A strong integration between these areas is essential. It is mandatory to launch application programmes in order to validate the tools and processes involved and to establish the needed connections to give the European users advanced access to the state-of-the-art technologies.

Special materials and equipment are required for the production of advanced chips. Progress in the production of such chips is fully determined by the availability of new production equipment. In this field too Europe has lagged behind. Not surprisingly therefore the programme proposes ways of remedying the weakness. If ICs are of strategic importance to Europe, then Europe must have the means to produce them. In a competitive world it would be unwise to rely solely on foreign imports. A strategic balance has to be reached whereby other countries need our supplies just as much as we need theirs. The programme contains many useful initiatives. However these need to be elaborated, extended and ordered in priority.

A major and accelerated effort is required on many fronts. New investment is needed, increased work force is required, so are new forms of cooperation. The JESSI-programme covers these requirements. The programme has been drafted by a broad range of European companies and institutes. It is self-contained and in the view of the council, if the operations described in the plan are carried out in cooperation, the stated objectives will be reached. However, the time-factor is of crucial importance. The plan must come into operation without delay if European firms are to catch up with their foreign competitors. The Green Book reflects the views of industry and other partners as of ultimo 1988. It must be noted that technology and markets change fast. Therefore, the programme will be subject to regular revisions regarding goals and priorities. This implies that at present the partners agree to the general scope and timing. Detailed commitments will be made at the time of presentation of definite work-plans, the so called "Blue Books".

The programme has to be considered as a framework. In some parts the actions and actors involved in the implementation are known precisely. In other parts necessary tasks are listed for which new partners have to be recruited. There are even parts where much room is left by the framework for a more detailed definition of projects or subprojects. The Planning Council expects that in the succeeding phases new partners will enter and new detailed tasks will be incorporated.

The principle decision about funding of the total programme has to be taken by the governments and the European Commission on the basis of the Green Book. The decisions about selecting and funding the various projects within the framework of JESSI will be taken later on the basis of the Blue Books. Blue Books can be prepared by participants who were already active in the planning phase and by participants who are new or partly new. To qualify for funding a project will have to satisfy certain rigorous criteria. It will have to fit into the overall plan, involve cooperation with partners and division of labour; in other words it must be a joint European initiative. The plan contains promising initiatives for new forms of cooperation. Funds will go primarily to those firms or institutes prepared to strengthen their cooperation activities or bring in new partners.

The Planning Council will shortly prepare a proposal for the organization of JESSI. A JESSI-board should be formed consisting of maximum 8 persons representing the major actors who execute the programme. Board members should have the confidence of the national governments, the EC and the major industrial and research participants. The board should have the assistance of a small office with full-time staff. The first task of the board will be to speak on behalf of JESSI with the governments and the EC. In the execution phase the board is responsible for the essentially intense coherence of the total programme. It has to approve the criteria to be applied in the sub-programmes for selecting actual projects. Before the JESSI-board has been formed the Planning Council will assume responsibility.

The extent of the board's authority, the way the board interacts with governments and participants in the plan, and the board's relations with management boards of companies and institutes, have still to be negotiated and worked out. It is likely therefore that the board's relations with the sub-programme management boards will not follow a uniform pattern.

The Planning Council herewith endorses the JESSI-programme. It is an integral programme, i. e. the four sub-programmes are strongly interlinked - without this linkage

sub-projects will not be included in JESSI - therefore no drastic changes, reductions or extensions can be accomodated without corresponding changes in other sub-programmes. The Council presents the plan to the governments and the EC, requesting them to take such measures that JESSI can be started on short term.

Companies and institutes are urged to express their commitment in terms of assignment of adequate manpower and funds in detailed work-plans. The programme should be in operation in 1989 in its entirety, since this is in the interest of the future well-being of the countries of Europe. ICs are here to stay but they need to be nurtured and propagated.

Munich, 1 February 1989
The JESSI Planning Council,

C. le Pair

(Dr. C. le Pair)
secretary

(Prof. ir. B.P.Th. Veltman)
chairman

0. Editorial

JESSI is an 8 years research and development program on silicon based microelectronics and its integration into systems.

The definition and planning phase for the JESSI Program started actively on 1st January 1988 and ends on 31th December 1988, as the EUREKA Project EU 127. It was the task in the definition phase to describe the technical goals of the JESSI Program and to develop a workplan and concepts for the realization phase. The execution will start in 1989.

The organization and task allocation during definition phase was regulated among the participating institutions and companies by the Cooperation Agreement of April 1988. The original number of partners increased very soon and has reached finally a level of 29. These research institutions and companies coming from 6 European countries (Belgium, France, Federal Republic of Germany, Italy, The Netherlands, United Kingdom) were all contributing to the planning work.

The planning was carried out by five teams, of which four section teams were appointed to the following chapters:

- that of chip production, in short "Technology",
- that of chip making "Equipment and Materials",
- that of "Application" of microelectronics,
- and "Basic and Long-Term Research".

The fifth team is working as a comprehensive Core Team.

A Planning Council made up of representatives of the participating companies and institutions attends the planning project.

The outline of the planning result is contained in this document.

Itzehoe, 31st December 1988

1. JESSI: A European Microelectronic Activity

1.1 Europe needs Microelectronics

The recent development of the technology-driven industries in the European community shows, that microelectronics is the key to competitiveness in the areas of data processing and communication systems, electrical engineering, precision mechanics and optics, automotive, and machinery industry. In 1987 more than 8 million people in the EC were working in these industries and realized more than 600 milliard $ of sales. The diffusion of microelectronics in these fields is a result of its dynamic development in terms of cost, and size reduction and increasing level of complexity and it affects strongly the performance and costs of the products and systems in which it is used.

Although the integrated circuit industry by itself is comperatively small today, microelectronics is a strategic weapon that helps to export high technology goods and services and thus secures jobs and the standard of living in the EC.

Within the next decade, the European electronics industry will become one of the largest manufacturing industries in Europe. In size, compared to ATT, IBM, NTT and NEC, the European system houses are comparatively small: as a consequence the growth and strength of Japanese and American microelectronics suppliers and users, which have large domestic markets for mass production, are a threat for the future of the European electronic industry. It places the European IC-producers and -users in a very difficult world position.

The world market for microelectronics will increase approx. 14 % per year until the year 2000, reaching approx. 160 milliard US $ with a 28 milliard US $ share for Europe.

The global competition between IC-makers is characterized by the aim to establish market position by market share, regardless of adequate rates of returns. It is notable, that already in 1987, Japanese IC-makers alone claimed nearly 50 % of the world market of ICs, followed by the US with a shrinking 39 %. For example the microprocessors as the heart of many products are still dominated by the US, while the markets for DRAM's or chips for videorecorders are dominated by Japanese IC-makers. The European IC consumption is more than twice as large as the

European production, thus creating a highly dangerous dependance in a key area of European industry. Especially, since the free access to US supply of advanced microelectronics may be influenced by global military aspects, that to Japanese supply by global economic interests. The fear is, that from a dependency in microelectronics, a dependency in electronics will follow, as the case of the computers and videorecorders e. g. shows.

Furthermore, the support by governments and governmental bodies in the US (e. g. by the Dep. of Defense or SEMATECH*) and in Japan (e. g. MITI, NTT, NHK) is focussing and strengthening industrial strategies in a way, that has no counterpart in Europe.

There are more arguments for strong European suppliers of microelectronics:
An increasing part of the performance of high-tech products is realized by the integration on a single application-specific or even customer-specific chip. So, a close and trustful contact between system manufacturer and chip manufacturer becomes ever more important: European users should have a healthy advanced European IC supply alternative.

Last but not least, chips have to be available at competitive costs: The highly volume-dependent cost structure of the IC-manufacturing process requires a high-volume manufacturing capability. The European electronics industry must grow considerably to play this important supply role in the European Community.

1.2 Microelectronics needs Europe

The European IC-Industry is vigorous and innovative, and demonstrates its willingness to keep pace with the rapid technological advance by enormous investments in research and production facilities. The same is true for the systems industry. But in respect to microelectronics they still require help by well defined European policies. This should include trade policies and the creation of European home markets. Furthermore, innovation support should include promotion of projects leading to new microelectronics manufacturing technologies, and to new advanced products integrating European application know-how in silicon chips.

* SEMATECH is a joint R&D activity of U.S. semiconductor and semiconductor production equipment manufacturers, which receives a subsidy from the U.S. government covering 50 % of its costs.

National support of microelectronics is provided; however, the size of assistance needed exceeds the nationally available funds; it needs to be complemented by a European effort. Further there is support within the ESPRIT framework, but no submicron CMOS technology is covered in broad, although this will be the dominating technology base of the three large European IC-makers in the 90s.

1.3 Technical Trends

Technology

If technological development worldwide up to 1995 proceeds at the same rate as in the past, the target figures listed in the following table could be achieved.

Expected Technology Data

	1990	1993	1996
Expected Technology	0,7 µ	0,5 µ	0,35 µ
Technology Drivers DRAM SRAM EPROM	 4 M 1 M 4 M	 16 M 4 M 16 M	 64 M 16 M 64 M
Transist./chip Memory Logic	 6×10^6 6×10^5	 3×10^7 3×10^6	 10^8 10^7
max. chip area (mm^2)	100	200	500

The transition to the component technology predicted for 1995 in which, for example, a 64 Mbit-memory (DRAM) could be produced, will require the application of fundamentally new solutions in essential sub-fields, such as cleanroom technology, lithography, wafer handling, packaging, bonding technology, etc.

At the same time, the cost reduction per circuit function will have to continue, although both the development costs per circuit, and the volume of investment for a semiconductor plant will increase at even higher rates. In this case, only new production technological concepts can insure the continuing innovative strength of microelectronics.

Application

As said earlier the use of modern microelectronics in the key industries is essential for the economic growth of the European countries. In the year 2000, on-chip system solutions will represent 50 % of the IC market. The strength of the European industry is its system know-how. In the future, translation of this know-how into products by means of standard IC's will gradually be replaced by integration of the entire system on an application-specific chip.

The growth dynamics especially in the fast growing area of application-specific circuits and systems will be strongly influenced by the question whether the specification and design process for the systemintegration of microelectronic components, including complex "systems on a chip", can be methodically and instrumentally mastered and quickly put into operation. Europe is therefore in a difficult situation, since the semiconductor industry has available its own design systems; however, the users of ICs (i. e. system and equipment manufacturers) are not sufficiently involved in the design process regarding their systems know-how. Consequently, the IC-users are looking for design system which support the entire system design process, which guarantee far-reaching independence from semiconductor manufacturers and which insure the protection of system know-how.

1.4 Definition and Goals of JESSI

The main goal of JESSI (Joint European Submicron Silicon) is to secure the availability of world-competitive microelectronics for the European industry. It is a proposed EUREKA research and development program for the technology of system integration based on silicon. The program has four main issues (Fig. 1.1):

Technology:

- Development of the basics and proving of a flexible competitive manufacturing technology for advanced system applications, to be available by the mid-90s.

The most advanced technical goal, within the framework of the JESSI Program, is a

CMOS-process with minimal structures in the 0.3 μm range. This fine structure range is achieved through intermediate steps at 0.7 μm and 0.5 μm. Each intermediate development involves the overcoming of technical barriers through innovative process steps. Reduction of manufacturing costs will be one of the most important targets. Memories (DRAM/ VRAM/SRAM/EPROM) are to be used as the technology drivers.

Application:

- Building up of flexible competitive system-design procedures and tools which are applicable throughout Europe, for the development of highly complex integrated circuits and their integration into systems, as well as their verification in advanced joint pilot projects in major areas of application.

The European industry has a world-wide leading position in solution-oriented system know-how in a broad range of application fields. The direct knowhow transfer into microelectronic systems realized on silicon is of increasing importance in comparison with the use of standardized integrated circuits. The competitiveness - today and in the future - in standard circuits (e. g. memories) will be determined largely by the smallest structure size, the highest integration density and production technique. The competitive strength for the development of application-oriented system solutions within this time frame, however, is to the largest extent determined by the availability of flexible process capabilities and design tools.

Within the framework of JESSI, application-oriented system-development tools will be tested in pilot projects (Europrojects), for example, in information processing, industrial electronics, automobile electronics and in the consumer sphere.

Equipment and Materials:

- Development of manufacturing equipment and materials for microelectronics in selected areas of the European supply industry.

World competitiveness for the European semiconductor industry requires immediate access to the most advanced manufacturing equipment. This can only be achieved by the support of a strong European supply in the areas of manufacturing equipment and semiconductor materials. The earliest availability of equipment and materials according to the technological developments in the semiconductor industry must be secured.

Close co-operation between European IC manufacturers and the European equipment/material suppliers is essential, as the case of Japan shows. Effective forms of co-operation will be developed within the framework of the JESSI program.

Basic and Longterm Research:

- Complementary applied research for the long-term future.

In order to secure Europe's future economic interests and to capitalize on its current strengths in microelectronics, JESSI's starting point must be a wellorganized interaction between industry and research institutes. Mediumterm goals of the "basic and longterm research" are to support the industrial development of ICs and their application, with feature sizes down to 0.3 μm, and to work out alternative solutions.

The contribution to JESSI may vary by country, depending on industrial and academic infrastructure and on national political and financial strategies. A balance has to be found in Europe between a uniform approach for JESSI for all countries and parties, and a participation according to national and sectorial interests.

JESSI Planning Group

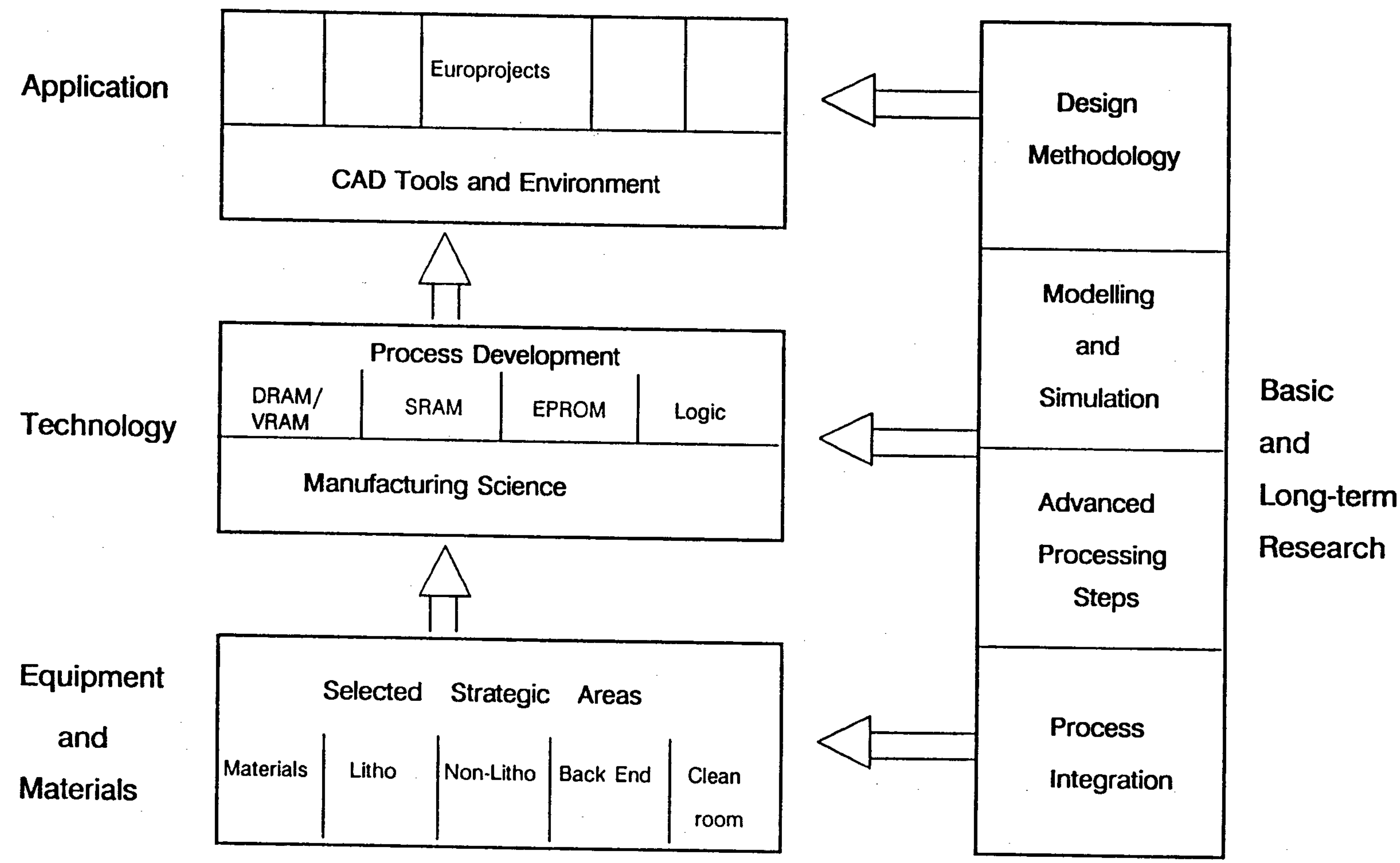

Fig. 1.1 JESSI-Program: Functional overview and structure of the European Microelectronic Program

2. Subprograms Outline

2.1 Subprogram: Technology

2.1.1 Actual Situation in Europe

Development and competitive manufacturing of state-of-the-art VLSI- and ULSI-circuits demand not only adequate process technologies but also refined or novel manufacturing technologies. Whereas european semiconductor manufacturers are excellent in some areas of process technologies (as demonstrated, e. g., in the MEGA project), an overall view of process technologies indicates gaps in comparison to overseas competitors. The situation is similar or even worse for manufacturing technologies. There is not much european experience when it comes to cost-efficient on-time operation of large wafer-fabs for submicron technologies. There is, however, a growing consensus among experts in the field that the present european ways of manufacturing integrated circuits are too costly and that manufacturing engineering should be treated as "true" science as is done in Japan and the USA (Sematech).

Philips, Siemens and SGS/Thomson (ST) all have large microelectronics R & D centers at their disposal which are capable of developing the process technologies of the future. Each company excels in a different memory type (SRAM, DRAM, EPROM for Philips, Siemens or ST, respectively) and uses its memory as technology-driver for other products. Process development for future memory generations therefore relies on the company R&D centers. Since the resources (Investment and Manpower) needed for the independent development of a new memory generation are forbiddingly large, cooperation on all possible levels, exploiting the large degree of synergy in subμm-technologies, could not only reduce costs and development risks but would also accelerate the overall program and therefore needs to be established or intensified.

Progress in manufacturing engineering, too, needs dedicated large-scale efforts. Again, cooperation in as many areas as possible without giving up the individual company strategy, is mandatory. Equipment-selection and -engineering, automation, clean-room technologies - including waste-management and safety issues - are areas which lend themselves to a high degree of cooperation and burden sharing.

Mastering memory technologies and the corresponding manufacturing technologies are the necessary (but not sufficient) ingredients for the competitive manufacturing of logic circuits. The strategic value of logic circuits in general - or ASICs in particular - for the european end users is high and expected to grow.

At present the degree of cooperation between the three IC manufacturers is not yet sufficient. Efforts to intensify cooperation already are under way; JESSI will be essential to increase the momentum towards a closer cooperation especially in logic-circuit technology.

2.1.2 Subprogram Goals

There are three major goals in the technology subprogram:

1) Development of submicron (down to 0,3 μm) memory generations (DRAM/VRAM, SRAM, EPROM) including the work needed to provide the necessary processing environment.

2) Development of logic technologies starting from todays 1 μm technology-base to utilization of the submicron technologies that will be provided by the memory projects. This development includes circuits derived as directly as possible from memory processes (e. g. microprocessors, gate-arrays) and more advanced circuits that contain process-modules not directly related to a corresponding memory generation (e. g. BICMOS or Logic with E^2PROMs).

3) Development of manufacturing engineering methods that assure timely and cost-efficient production of present and sub-micron circuits on 150 mm and 200 mm wafers.

The pace of the necessary activities is set by the world-market which is dominated by overseas competitors. The participating companies are forced to use the best equipment available, regardless of its origin or a resulting partial dependence on overseas equipment suppliers. These companies, however, would like the european equipment makers to be competitive on the world market and therefore are comitted to a close cooperation with the european equipment industry within the framework of JESSI. The goal is to decrease the dependence on non-european equipment; interaction with selected equipment manufacturers is

therefore a necessary activity connected with the technology subprogram.

Research and development of 0.5 μm memory processes has already started in all three companies. Naturally, they are based on the preceding memory generations and take place in the respective R&D centers. Since company histories are different and the present 0.7 μm CMOS processes are different, the 0.5 μm processes cannot be fully unified in the future. This is unavoidable because of differing circuit requirements (e. g. very different specifications of thin dielectrics for DRAM, SRAM and EPROM). Cooperation on the 0.5 μm process and in particular on the 0.3 μm process, however, is intended on processmodules and corresponding equipment (e. g. planarized deposition of intermetal dielectrics), on device and process modelling, on reliability issues, on packaging, and on many aspects of manufacturing engineering.

Whereas the potential of this cooperation is large, it is considered mandatory that each company will retain the ability to process its wafers in its own R&D center.

Research and development work for 0.3 μm processes is still in its infancy. All that can be stated so far is that even stretching many processes and materials to their utmost limits will not be sufficient; a sizeable number of new process modules and materials must be found. A larger degree of cooperation appears to be possible; ideally a common "back-bone" CMOS process could be established that each company could use for its own purpose. By adding specific process modules to and by minor modifications of the back-bone process, each company could derive its specific product spectrum (including Logic) and thus still remains a competitor in the market place.

Logic circuits follow the corresponding memory generations with a time-lag of 2 - 3 years. In a first step, a memory process that has demonstrated stability, high yield, and high reliability will be used for the processing of logic circuits with as little process module modifications and additions as possible.

For a SRAM derived Logic this may imply no more than another layer of metallization; for DRAM or EPROM derived Logic a few specific process-modules may have to be added to a simplified memory process because of different electrical requirements. The potential for cooperation is similar to what has been stated above, with the added possibility of know-how exchange for logic-specific process modules.

In a next step, the logic circuits thus established will serve as a base for more sophisticated products. These can be envisioned as logic circuits that incorporate "options" in the form of one or more specific functional units. Examples could be bipolar transistors (BICMOS) for, e. g., power applications or E^2PROMs for, e. g., "smart cards". Whereas these options may already exist as stand-alone products, their incorporation into a logic design and process-flow is not straight-forward and will require specific and sometimes extensive work.

The development goals that have been described and set into their contexts might be considered to be met as soon as engineering samples of memories or of Logic-demonstrators are functional on time. Whereas this would be true for the respective process development, the achievement of only these goals would not address all objectives of the Subprogram Technology. An equally significant goal must be to demonstrate in suitable pilot-lines (including wafer processing, assembly, and testing) that products can be manufactured in such a way that milestone and cost targets are met. These targets may be widely different, e. g. for DRAMs, and full-custom ASICs: For DRAMs mass-production at competetive costs and therefore high yields are necessary; process cycle time and flexibility is of secondary importance. In contrast, full-custom ASICs require short process-cycles and high flexibility, whereas yields and cost considerations beyond a certain level could be of secondary importance. Addressing these conflicting requirements without sacrificing a unified approach to manufacturing engineering is a demanding task that requires new concepts and ideas.

Issues that require extensive work, especially because 200 mm wafers have to be taken into account, are, e. g., equipment engineering (starting with translating process requirements into equipment specifications and ending with improving and maintaining working equipment); automation (starting with computer - aided lot tracking and ending with a mostly automated factory) and clean-room concepts (selecting between radically different approaches as, e. g., large "super" clean-rooms or localized clean-room concepts such as SMIF).

Manufacturing must be competitive. This means optimizing cost, yield, cycle time, process flexibility, equipment utilization and labour productivity calling for an appropriate level of automation. This level will be a moving target towards full automation which presumably will never be reached. Automation is limited by equipment reliability and process stability, as well as the need for flexibility.

Possible benefits also have to be carefully balanced against automation-specific

costs, as demonstrated by the failure of existing fully automated facilities.

Even with optimal automation, the production of integrated circuits will require a sizeable human work-force. This work-force must not only be highly trained and willing to work in shifts (7 days a week), but must identify itself with the task in an unprecedented way. An integral part of manufacturing engineering is to specify the actions necessary to assure adequately trained human resources.

2.1.3 Subprogram Structure

The Subprogram Technology consist of 5 projects. All projects are structured into project sections (e. g. Design, Process, and Support for the DRAM/VRAM-project) which are in turn partioned into subprojects. The subprojects (e. g. Lithography) define the work to be done, the relation to other projects/subprojects and the major mile-stones.

1) DRAM/VRAM:

This project contains all the work necessary to obtain engineering samples of 16M and 64M dynamic random-access memories and "Video"-RAMs (which are DRAMs with a special design).

2) SRAM:

This project contains all the work necessary to obtain engineering samples of 4M and 16M static random-access memories.

3) EPROM:

This project contains all the work necessary to obtain engineering samples of 4M, 16M and 64M electrically programable read-only memories.

4) LOGIC:

This project contains all the work necessary to obtain engineering samples of logic circuits as demanded e. g. for the activities of the subprogram Applications. It encompasses basic memory based logic as well as Logic with Options. It is a project in which Philips, Siemens, and SGS-Thomson will share resources and burdens as far as possible by taking into account their respective product strategies.

5) Manufacturing Engineering

This project contains all the work necessary to insure timely cost-efficient pilot production of memories and logic leading to product qualification and subsequently economized process. It is a project in which the partners pursue their production strategies while using results and know-how generated in joint efforts.

2.2 Subprogram: Equipment and Materials

2.2.1 Actual situation of the European Equipment Industry

For the time being the European equipment industry shows with a few exceptions a very weak position worldwide. The equipment market is dominated by US-manufacturers with a steadily increasing market share by Japanese companies. In order to be profitable in the equipment market showing a fierce competition, the Europeans have to operate worldwide because there own homebase is much to small.

The prime reason for this situation lies in the relative position of the European IC-industry itself, which in the past was lagging behind the most advanced IC-technology. There was therefore no ground for having a strong equipment industry around. All the equipment required was easely available from outside, because there was of course no need to exclude the European companies from aquiring this equipment neither technically nor commercially. There was no general thrust from the IC-industry to make a cooperative effort in building up a competitive equipment industry in Europe. The close cooperation however is the indispensible prerequisite for developing high quality production systems for IC-fabrication. The strong efforts within ESPRIT and the MEGA-project led to a shrinking gap between the US/Japanese and European companies in specific areas (e.g. memory chips) requiring the most advanced technology. With commercial success the competition with the Japanese and US-IC-manufacturers will get rougher and the probability not to have the most advanced equipment available from those countries in time will increase with the progress of the European IC-manufacturers. The situation for the home market of equipment makers will change positively. First the homebase will broaden and secondly the immediate access to the most advanced equipment will gain strategic importance with growing strength of the European IC industry.

The fact, that the equipment industry is one of the strategic elements becomes evident from the activities within the US effort SEMATECH. In a strategic approach the European IC-industry will also have to influence the development of innovative equipment.

Despite the favourable development of the equipment market, in Europe the base will still remain rather limited, therefore it is a must for the equipment industry to operate worldwide. With increasing complexity of the advanced equipment the R & D-costs as well as the development time will increase dramatically. This financial burden can not be carried by the still relatively small European companies themselves. To cope with the worldwide competition especially because of the strong fluctuation in IC-industry the companies have to have adequate financial and technological resources.

There are not only chances for the larger equipment makers. There will be also chances for smaller manufacturers of R & D-equipment as well as of subsystems (e.g. Rf-power supplies and measuring equipment).

In judging the actual situation in Europe it turns out that the research base is fairly well established in Europe. But no R & D-infrastructure is available to test and optimize innovative prototypes. Also for the decisive step in equipment development, that means the testing and optimization phase of the equipment in an IC-fab-line, the preconditions were not very favourable in the past.

One of the main issues during the JESSI-program has to be therefore the improvement of the infrastructure for developing prototypes (strengthening of specific centres of excellence e.g. AIS/IFA, Leti, Imec) as well as the establishment of a close cooperation between the equipment and the IC-manufacturers for the development of high performance production systems.

2.2.2 Role of the "Equipment and Materials" within the JESSI-program

Deriving from the prime JESSI goals, the role of the subprogram "Equipment and Materials" within the JESSI-program is twofold:

Firstly the subprogram "Technology" has to be supported which aims for the production of 16 Mbit and 64 Mbit memories respectively. To ensure that the equipment being developed within the JESSI program fullfills the technological requirements for the 16 Mbit/64 Mbit production the IC-manufacturers have to have a strong influence on the development of this kind of equipment.

Secondly JESSI aims to build up a solid base of European equipment manufacturers also for the time beyond the JESSI-program. This is specifically valid for all those systems which promise a potential of application for the future (e.g., multi-chamber processing). In order to build up a sound equipment industry in Europe a long term strategy should exceed the period of the JESSI-program. From the present point of view it doesn't make sense to tackle the whole equipment market. In order to take full advantage of the limited resources within Europe the development of manufacturing equipment should be focussed on selected areas.

The stronger cooperation between equipment makers and IC-producers foreseen within the JESSI program will also create a better framework for the planing of production and marketing schemes for the equipment and material makers.

2.2.3 Subprogram structure

Special attention has to be given to the prompt availability of equipment with 200 mm wafer capability.

In identifying the important areas in which the European equipment manufacturers may be active the following criteria have been employed:

- strategic importance (key systems)
- urgent need of the IC-industry (no satisfactory systems available yet)
- worldwide competitive situation
- specific technological strength in Europe
- fields of new emerging, highly innovative systems

The subprogram consists of 5 project groups (e.g. Lithography oriented equipment). All the project groups are subdivided in projects (e. g. optical lithography) which in turn are partitioned into various subprojects (e. g. optical lithography: new optical materials, reticle generation, new DUV-technology). The projects as well as the subprojects do not define the detailed work to be done but rather the important areas to be dealt with in order to develop a piece of equipment successfully.

1. Automation/clean room:

This project group contains automated process equipment (automated wafer handling, data interfaces etc.), equipment for automation (raticle storage units etc.), computer control systems (CAM/CIM) and clean room technology.

2. Non-lithography equipment:

This project group contains the equipment development which immediately supports the technology for the 16 and 64Mbit generations (e. g. furnace oxidation, rapid thermal annealing, ion implantation, etching etc.) as well as those equipment developments which will probably not be used as production equipment within the JESSI framework but which offer a high potential for the future.

3. Lithography-oriented equipment:

This project group is also divided in activities supporting immediately the 16/64Mbit-technology (optical lithography, resist processing, optical CD metrology etc.) and in those projects which will supply alternative options for existing lithography tools (X-ray lithography, electron beam lithography).

4. Back end processing/testing:

This project group consists actually of two distinct projects (assembly and testing) with a rather large number of subprojects (assembly: dicing, die attach etc., testing: IC-tests, burn-in etc.). The projects within this project group are primarily directed towards an immediate application in the 16 and 64Mbit technology. The main issues are the reliability and performance of the equipment, the contamination caused by the materials used (ions, metals, alpha particles) as well as the flexibility to cope with the upcoming ASIC-IC-technology.

5. Materials

This project group contains the development of high quality silicon base material, of process materials (photo resist, gases, wet processing chemicals), of the packaging materials (plastics, ceramics) as well as of metals and quartz. Developments in this area are supporting the 16/64Mbit-technology

directly and will therefore be exploited within the JESSI framework.

Within these topics the contributions entail the actual state of the art (including the competitive situation), the actual technical and commercial problem areas, the nomination of technical issues to be tackled in future projects. In this state a differentiation was made between short, medium and longterm strategies. A ranking system 1 to 3 has been applied (either for the immediate support of the IC or for the success of the equipment industry).

2.2.4 Equipment development

The development of a piece of equipment normally exhibits three clearly separated phases (material development is different). The R & D oriented first phase deals mainly with new and innovative concepts leading eventually to a laboratory type system for feasibility studies. In this stage primarily a cooparation between R & D facilities and equipment manufacturers is required. The IC-industry sets the technological frame, but normally there will be no strong involvement of the IC-manufacturers in the single projects. This phase is generally characterized by a large number of smaller projects.

The backbone of a successful equipment development program is a close cooperation between the equpiment manufacturers and the IC-industry. In the first two stages of the equipment development the involvement of European R & D facilities (centers of excellence) will support this cooperative effort.

In the second phase promising equipment concepts will be continued towards a first prototype system by the equipment manufacturers. At the end of this engineering phase a mature prototype system which is able to be implemented in an IC-pilot-line has to be provided. There will be cooperation between R & D (special subtasks), the IC-industry (providing the specifications and technical guidelines) and the equipment manufacturers (developing the technical concept and the system design). In this stage there may be still more than one concept heading for the same technological goal because it is often impossible to asses the performance of the specific concept within this phase. For some strategic important projects (e.g. DUV-stepper) there may already be a strong commitment of the IC-manufacturers.

In the third phase, however, a strong commitment is the necessary precondition for the development of a mature piece of production equipment. The evaluation and the optimization of those systems required have always to be carried out in

direct conjunction with an industrial key customer. In this context the IC-industry is selecting appropriate prototype-systems showing the best preconditions (maturity, specification, etc.) for further optimization towards the final production system.

2.2.5 Material development

Beside the silicon base material which has always been recognized as the key for a successful fabrication of integrated circuits the process materials like photo-resist, gases and the packaging materials (plastics, ceramics, etc.) as well as metals and quartz etc. gain rapidly importance for the semiconductor process technology. One of the main issues for future VLSI technology concerns the extreme low level of contamination and particulates which are acceptable for a reasonable yield. The materials addressed in this section do not include the materials being used in the equipment (e. g. gas tubes, valves, containers, electrodes) which of course have also a very high importance for the process technology. These materials, however, are considered as being part of the equipment development. Unlike the equipment development there is no clear separation between basic research and final product development in the materials sector. Therefore the strong involvement of the IC-industry in the materials development is required right from the beginning. That means all projects running in this section should be based on a very close cooperation between the materials manufacturers and the IC-industry.

Providing very pure materials is, however, only the first step in having the cleanest material available in the process. There should be, therefore, also an intensive cooperation between the materials and the equipment manufacturer in order to analyze the interaction between the process materials and the specific parts of the equipment (containers, tubes etc.) and to optimize those subcomponents for retaining the high degree of purity of the materials up to the point of use.

Another strong interaction with the analytical part of the basic research activities is required for developing measuring methods for very low contamination levels not yet available. In order to provide the highest possible quality of the silicon material (defects, material inhomogeneities etc.) the crystal growth equipment has to be improved drastically. The transition from 6 to 8 inch which is likely within the JESSI-project calls for new concepts in the crystal growth equipment. Therefore the development of this piece of equipment has been implemented as a indispensable prerequisit for providing high quality silicon

material in this project area.

2.2.6 Rules for the selection of projects

Project proposals in the first phase as definited earlier will primarily focus on sub components (in-situ measurements, materials, etc.) or on new concepts (photo-induced processes, new process-chemistry etc.). The JESSI-program provides the frame for the project.

In the second phase a first prototype has to be developed fit for IC-manufacturers to operate in a pilot-line for test and evaluation. Only those projects have to be selected which fullfill the specification set by the IC-industry or at least fit in the future technology trends also judged by the IC-industry. There may exist, however, different project proposals aiming for the same goal. In the same way as the IC-industry has to be free to look for help outside the European frame-work (in case of no adaquate European base to develop the specific most advanced equipment) the equipment manufacturers have to have the opportunity to cooperate with IC-manufacturers outside the European community in order to push a promising concept which may not fit completely in the actual philosophy of the European IC-manufacturers.

In the third phase there are strict selection rules (may be similar to SEMATECH) which promote the best prototype system towards a mature production system.

The exact rules for making a fair selection have to be established later on.

Apart from the criteria mentioned in 2.2.3, the following general criteria have to be met:

1. Technical prerequisites:
   - high innovative concepts
   - sound technological strength within the companies
   - sufficient R & D resources within the company

2. The commercial prerequisites:
   - sufficient financial resources
   - worldwide service/marketing
   - limited strength of the competitors worldwide

2.3 Subprogram Application

2.3.1 Present situation in Europe

To design complex systems, the user encounters a panorama of isolated, non-compatible tools. These do not cope sufficiently with the existing complexity. Moreover their operation requires intensive training.

Tools of today are mostly either captive, i. e. not available in public domain, or come from US-companies. Long term support and maintenance are often not guaranteed. And, what makes the situation worse, standards and common libraries do not exist.

What is lacking -above all- in Europe is the spirit of TOGETHERNESS which is typical for Japan Incorporated. Japanese companies compete strongly amongst each other, but not before having shared in the effort to conquer a new market for Japan.

Many semiconductor manufacturers, especially in far east, are integrated into vertically structured system houses. Therefore, careful attention must be paid to defining user/producer interfaces in order to guarantee protection of the users know-how.

2.3.2 Subprogram Goals

For the development of the future design environment, it is necessary to align the existing European potential and to use it toward achievement of the user's goals. The design environment must exhibit at least enough strength to realize systems of that complexity as mentioned in the technology subprogram. This has to be done from the conception phase of the system all the way to the finished product. This requires both the mastering of technology-based options as well as the completion of various system designs, based on different technologies, in as short a development time and as cost effective as possible. JESSI should encourage the creation of a European CAD software supply.

For the use of design capabilities and the meaningful application of IC's it is necessary to have trained specialists. This is also the case for the development of application tools. The training aspect, therefore, is an important issue.

There are two major goals of the subprogram "Application".

- Building up of flexible competitive procedures and tools for the development of highly complex integrated circuits and their integration into systems.
- Developing prototypes of microelectronic systems which may serve as vehicles for specification and evaluation of CAD systems using advanced technologies in strategic application areas.

To achieve this goal a number of projects have been defined and are grouped into three main topics:

CAD Tools and Environment-Projects have to provide a powerful and competitive CAD-System. This system has to be configurable in such a way that big companies as well as small and medium sized ones are able to compose their special toolbox with moderate costs. The results are supposed to be evaluated by users, e. g. in Europrojects

Europrojects aim for bringing up prototype systems from which requirements for essential new tools beside the general ones from above will be derived. They also serve as test vehicles for tools, environments and system design methods.

Education and Training will have to provide an increase in the number of skilled system design engineers and CAD personel. Education and training programs in universities and technical colleges will focus on the needs of small and medium sized companies. The project JESSInet will be set up to facilitate communication between the partners, and must be set up during start- up projects. The project European CAD Initiative will yield an organization, that pushes standardization, balances the influences and coordinates the decentralized actions of the participants.

2.3.3 Subprogram Structure

2.3.3.1 Project Group Support

Besides the technical Project Groups there exists a set of projects that handles more general issues like

- organization,
- communication
- education and training.

Because of the decentralized realisation of the subprogram "Application" a tight coupling of all activities is required.

An organizational structure (working title ECI = European CAD Initiative), that balanced the influences of all participating companies and institutes, has to ensure the outcome of commercial, powerful and competitive CAD systems, based on worldwide standards. ECI will be responsible for all aspects concerning standardization and interfaces (definition/selection, promotion, coordination, initiating, and control). The ECI may also give advice to JESSInet, and education and quality.

From existing experience in individual companies and institutes it has become clear that a network is essential to improve a fast and easy access and distribution of common information (TOGETHERNESS).

Some levels of education and training in the area of electronic system design, VLSI design, tool management and software engineering will have to be supported by the JESSI program. Next to regular courses in universities and technical colleges training programs on JESSI CAD tools and the underlying methodologies will have to be provided to the industry, especially to the small and medium sized companies. These activities should result in an increase of the number of skilled CAD personel (designers and software developers) and electronic system engineers.

2.3.3.2 Project Group "CAD Tools and Environments"

The design and development of complete systems must be supported. This task becomes more complicated as systems may be composed of different levels of implementation (physically e. g. boards and integrated circuits), and additional problems arise at the interfaces between these levels. Furthermore, system design has to cope with a variety of different target technologies (e. g. for digital or analog applications, for optical/ magneto- mechanical interfaces) and target architectures (ranging from multiprocessor networks down to glue logic in a variety of applications). Additionally, all levels of abstraction should be covered in the design process.

System design addresses all these areas. An attempt to overcome at least some of the related problems requires a common tool environment. Thereby,

standardization of interfaces is urgently needed as well as an open design system which allows the easy integration of new tools. The direct application of general tools as well as the specification of special ones within Europrojects guarantees the necessary feedback for tool development.

Within this Project Group an open, integrated environment and CAD tools will be developed which

- enable economic, fast, reliable and efficient system design in a design environment as independent from technology as can be.
- are capable to handle 1996 complexities/technologies in system design.

To meet these objectives standardization must be applied as far as possible. This has to be done in accordance with the world-wide progress.

One general JESSI environment will be developed which supports various design strategies and contains all major tools and services. The base system should satisfy several fundamental requirements:

- Ability for integration of tools via binding standards and open interfaces.
- Portability via standardized reference systems.
- Openness towards current and future tools, available on the market.
- User-friendliness, with a generic kernel of a user interface system and a universal data management.
- Configurability for various levels of implementation (IC, PCB, systems ...), methods and areas of application.

The delivered environment should be a basis for the development of more specific environments for particular applications.

JESSI CAD systems will have to support users in the whole range of application from small and medium sized companies, which may work on the specification level only, to companies or institutes which make the physical layout by themselves, tuned to the latest state of the art in semiconductor technology.

The evaluation and validation of this environment is performed within "Tools and Envrionment", " Europrojects" and additional system design activities.

The work to be done within the area of design tools is concentrated within six projects, each structured into a set of subprojects:

1) Environment and Standards
2) Framework
3) Languages and Editors
4) Validation and Verification
5) Test Generation and Design for Testability Support
6) Synthesis, Optimization and Analysis

2.3.3.3 Project Group Europrojects

A Europroject is a combined effort of European companies in the first place (but institutes may participate as well) in some strategic application area and aims at prototype systems. These systems are developed up to a level that end-users (i.e. customers) can be asked for validation.

Aside from general CAD-tools, application specific tools and environments will be developed where needed.

The prototype systems serve as test vehicles for tools, environments and technologies being developed.

The collection of proposals given by different companies and institutions so far (cf. MATRIX, Fig 2.1) should be looked at as being a profile of the current interests between JESSI-partners. Some may start as early as by summer '89. Some clustering and/or merging between partners will be needed.

Major changes must be expected from negotiations between proposing individual institutions up and until the time the participants commit themselves to detailed project proposals.

Criteria for selection will be suitability to:

- Contribute to the competiveness of the European users.
- Provide the right CAD requirements for the nineties.
- Serve as pilot designs for testing the CAD-tools and environments to be developed.

Detailed Europroject proposals have to show to what extent the JESSI environment is used and evaluated and which of the special CAD-tools will be public within the JESSI domain. A classification scheme which complies with these two conditions has to be worked out.

Europrojects: Matrix of Interest

Fig. 2.1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	16	17	18	19	20	22	23	24	25	26
FhG		—	×			—		×	×	×	—	×												
SEL/ALC.	×		×	×		×			—	×													—	
Löwe Opta	×	×		×	×	×																		
ABB			×						×	×		×	×											
BMW					×																			
Bosch			×	×	×	×			×															
Bull								×	×									—	—					
AEG/Daimler			×	×	—	×			×	×		×			×									
Krupp Atlas		—				—	×	×	—	—				—			—							
Nokia	×		×	×					×															
Philips	—		—	×	×	×		×	—	—		×	—	×	—	—	—	×	×	×	×	—		
Plessey				×					×															
Siemens	×		—	—	—	×	—	×	—	×		×				×		×	×	×				
Thomson	×	×	×	×		×			×	×														
ES2									×															
GMD							×	×	×	×				—										
ST	×		×	×	×		×		×	×		×												
Alc./NL																				—				
PTT-Onl									×	×														
IOP-IC									×															×
TPD-TNO									×	×														×
TU-D						×					×			×							×			—
OCE						×				×											×			
Dutch CTI	×								×		×													×
Sierra									×															
T-Univ.Eindh	×			×					×		×			×										—
Uni Twente									×		×													
Nixdorf																								

additional partner

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.
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1 High Definition Television (HDTV)
2 Digital Controls for High Res.Display
3 Mobile, Automatic Cellular Radio/DAB
4 ISDN Components
5 Automobile Electronics
6 Image/Voice Recognition/Processing
7 Microprocessors/Microcomputers
8 One-Chip Work Stations/Risc
9 Asic Basic Building Block Family (including ESPRIT-IDPS projects)
10 Signal Processors
11 Small Medium Industry Support
12 Industrial Electr./Analog Interf.
13 Digital Servo's
14 Novel Architectures Comp/Proc.
16 Nidas
17 Consumer Fax
18 CHC-Cad
19 Risc Embedded Controllers
20 Risc Imb. Proc. Stand. Funct.
22 Telecom-Switching
23 Graphics
24 CD Interactive
25 VID/AUD. Codex 64 KBS Videophone
26 Inductive Fault Aval. A.O.

additional suggestions . . .

— = Initiative (proposals/initiators)
× = Participants (interested parties)

2.4 Basic and Long-term Research

2.4.1 Subprogram Goals

The Basic and Long-term Research (BLR) subprogram goals could be defined as:

1. Support the European micro-electronics industry with research results to ensure that
   - the IC manufacturers can reach their goals of 0.3 μm structure width, 500 mm^2 chip area and 10^7-10^8 transistor complexity in the pilot production in 1996 and beyond,
   - a growing field of materials and equipment suppliers will reach a strong competitive position.

2. Broadening of the basis of the micro-electronics industry by developing alternatives to improve on and enhance established technologies and to overcome unforeseen future technical and economic bottle-necks.

3. Assure long-term continuity for the micro-electronics industry by developing new methods and technologies to be exploited economically after 1996.

The BLR-projects are all closely connected with other JESSI-projects. The BLR-projects are partitioned and defined such in order to optimize internal coherence within JESSI.

Research tasks will be carried out either by groups in industry, institutes or universities. Final decisions have to be made later on the basis of the detailed proposals. The overall quality of proposals and proposers will be the dominant criterium for participation.

The goals of the projects are split into "research support", "research alternatives" to the main stream and "long-term research" (even beyond 1996), indicating both a time frame and a degree of risk.

Research in the first two categories needs a tight cooperation between research groups and with industry and must be guided by industrial partners. Long-term research implies however an increased risk factor and permits a more flexible and open structure. Participation of the academic institutions will be dominant in this case and should be based on an open call for proposals. Many research tasks

cannot be described very tight at the moment and furthermore priorities and concepts might change during the years of the JESSI program. It is important to note that the major part of the research activities requires participation of research centres with a critical mass of qualified staff.

Taking into account the number of autonomous institutions that will participate in JESSI, the project management must be strong.

2.4.2 Structure

The subprogram Basic and Long-term Research (BLR) is structured in the four project groups indicated below, defining 14 projects.

Design Methodology

1. Methods and Tools for ULSI Design
2. System Related Circuit Design
3. Technology Related Circuit Design
4. Methods and Tools for ULSI Chip Design

Modelling & Simulation

5. Process and Device Modelling and Simulation
6. Circuit Simulation

Advanced Processing Steps

7. Submicron Lithography
8. Etching
9. Ion Implantation and Thermal Processing
10. Advanced Deposition Techniques

Process Integration

11. Novel Devices and Structures
12. Interconnection
13. Assembly and Packaging
14. Analysis, Testing and Measuring

The 14 project descriptions, resulting from a bottom-up approach of experts in the field, are given in the Detailed Project Descriptions Sections; for further details appendices are available.

The project group tasks are the following.

1. **Design Methodology**

Maximum exploitation of JESSI technology through the design of complex ULSI systems ranging up to 10 million devices will not be possible by mere evolution of the existing design methods and tools. In order to overcome the bottleneck in design time and the increasing probability of fatal design errors, there is a need for the evaluation and development of new principles for the logical construction, synthesis and verification of ULSI system design.

A formal methodology for logical design will be followed up in the project Methods and Tools for ULSI System Design as an exploratory long-range complement to the work of the subprogram Application. This will be accompanied by exploratory experimental work in the project System Related Circuit Design, which aims at investigations for the improvement of systems building blocks and communication strategies. Demonstrator chips planned will be dedicated to studies of new architectures, technology features and parasitics, and the problems encountered with the probable change of standards like supply voltage and logic levels. Hence, this work is a long-range complement to the europrojects.

The physical design will have to be treated also in its technology related aspects. The goal is to improve existing and to develop new basic circuits. For example parasitic effects have to be studied and eventually utilized. This allows in an early stage of development a choice of technology directions and the recognition of constraints that must be accounted for in the development of CAD tools. A topic of strategic interest is an early basic design work in preparing concepts for the 64M memory generation, which will be adopted and continued by the technology group in the middle of the project.

Methods and Tools for ULSI Chip Design will be necessary to link both physical and logical design at a scale of up to 10 million transistors, a goal that is beyond the possibilities of existing tools. Work will be partly done on request of the subprogram Application, partly as an exploratory long range extension.

2. **Modelling and Simulation**

The development of processes and devices requires fast, accurate and reliable Process and Device Simulation Tools and adequate Process and Device Models.

The research will start with the development of new computational methods and new program architectures, exploiting the modern computer capabilities (parallel processing). In a more mature stage of the project, the process and device simulation research has to concentrate on the development of user friendly simulation tools with optimization facilities and good interfacing. For the development of adequate models good physics will be of crucial importance.
A new Circuit Simulator will be required for design verification of the new JESSI generation circuits. The main goal is to improve the performance (speed and complexity) of circuit simulators by a factor of 100 - 1000. BLR will work on new methods based on novel circuit partitioning algorithms and device optimization in the critical path. Mixed mode simulation has to be included.

3. Advanced Processing Steps

The research in this field consists of four projects: Submicron Lithography, Etching, Ion Implantation and Thermal Processing and Advanced Deposition Techniques. The first part of the project Submicron Lithography is concerned with deep UV lithography (193 nm) and supports the activities in other subprograms (Technology, Equipment). X-ray lithography is actually considered as being the most important alternative to DUV-lithography. An industrial decision has to be made after 3 to 4 years for a possible transfer into an industrial environment. The other subprojects will supply alternative options for existing lithographic tools like electron beam lithography, both the scanning and projection type, and charged beam projection. These alternative solutions are back up options for the lithography in the 0.3 μm range, and for even smaller dimensions. Attention will also be focussed on advanced inspection and metrology tools.
In the Ion Implantation project research will be carried out to support the improvement of current ion implantation techniques. Special attention will be given to novel high energy ion implantation techniques and doping profile engineering. These subprojects will provide alternatives for current devices and processing. Two other subprojects are intended to supply urgently needed data for novel thermal processing and to increase the basic knowledge in the ion implantation field.
The subproject Etch Process Induced Defects in the Etching project is intended to provide support for an improvement of radiation damage during processing in etch plasmas. The other subproject, Laser and Ion Beam assisted Etching, provides possible alternatives for the present day plasma etching. The project Advanced

Deposition Techniques will provide alternatives for the present day gate dielec trics and support for the metallization projects, both in Technology and Basic Research. Important long range aspects are covered in the subproject Epitaxial Layers where novel processes for the low temperature deposition of epi-layers and selective processes will be investigated.

4. Process Integration

The development of high-density ULSI-circuits with potential applications ranging to the end of this century will ask for the development of Novel Devices and Structures. Improvement of conventional device performance may be achieved by application of silicon-on-insulator structures, novel gate dielectric materials, or by low-temperature operation. Novel device structures for example for memories have to be investigated (e.g. vertical integration, non-volatile cells and ferro-electric RAMs). On a somewhat longer term, stacking of devices to achieve 3D integration offers an interesting alternative. To ensure the long-term continuity novel devices will have to be studied, to achieve improved device performance by a mechanism other than down scaling.

The demands on Interconnection will increase significantly in the larger area, higher packing density circuits. Research efforts will focus on improvement of materials (low resistivity, high critical current, ...) and technologies (selective deposition, self alignment, planarization). These efforts will be accompanied by activities on testing and characterization, and on modelling and simulation, to open the way to highly complex, reliable multilevel interconnection systems. Assembly and Packaging is already at present responsible for an important part of the total costs of a chip or system. Novel technologies like laser soldering, chip to chip interconnection, new cooling schemes, to name only a few, will be studied.

The research project on Analysis, Testing and Measuring provides the diagnostic tools to be able to have feedback in every stage of the production process. Micro-analysis, non-destructive in-line techniques, electrical evaluation and novel testing methodologies are the key issues for research in this field.

3. JESSI Program Milestones

3.1 Overview

The workplan of JESSI has been organized around major milestones which will give competitive position to the European microelectronic industry.

The key dates for JESSI are related to the availability of competitive technology processes and memory products on one side and of powerful CAD system for microelectronic system design on another side.

For the semiconductor makers the first major milestones correspond to the fabrication of the 1^{st} silicon which will be obtained after 2 years (end 90) for the 0,5 μ CMOS and after 5 years (end 93) for the 0,3 μ CMOS. One year later Multimegabit Memory Engineering samples will be delivered to selected users and preliminary design rules will be available for logic product design. In term of automation and manufacturing science the implementation of new systems will be done step by step in order to demonstrate at the end of the project complete integration of flexible automated manufacturing lines.

The next table (fig. 3.1) shows the overall planning and milestones schedule.

For the system houses, the earliest availability of Design Rules and powerful CAD Tools for the anticipated product design complexity will be decicive. Logic product designs in 0.5 μ technology are to be supported by 1993, and in 0.3 μ technology in 1996.

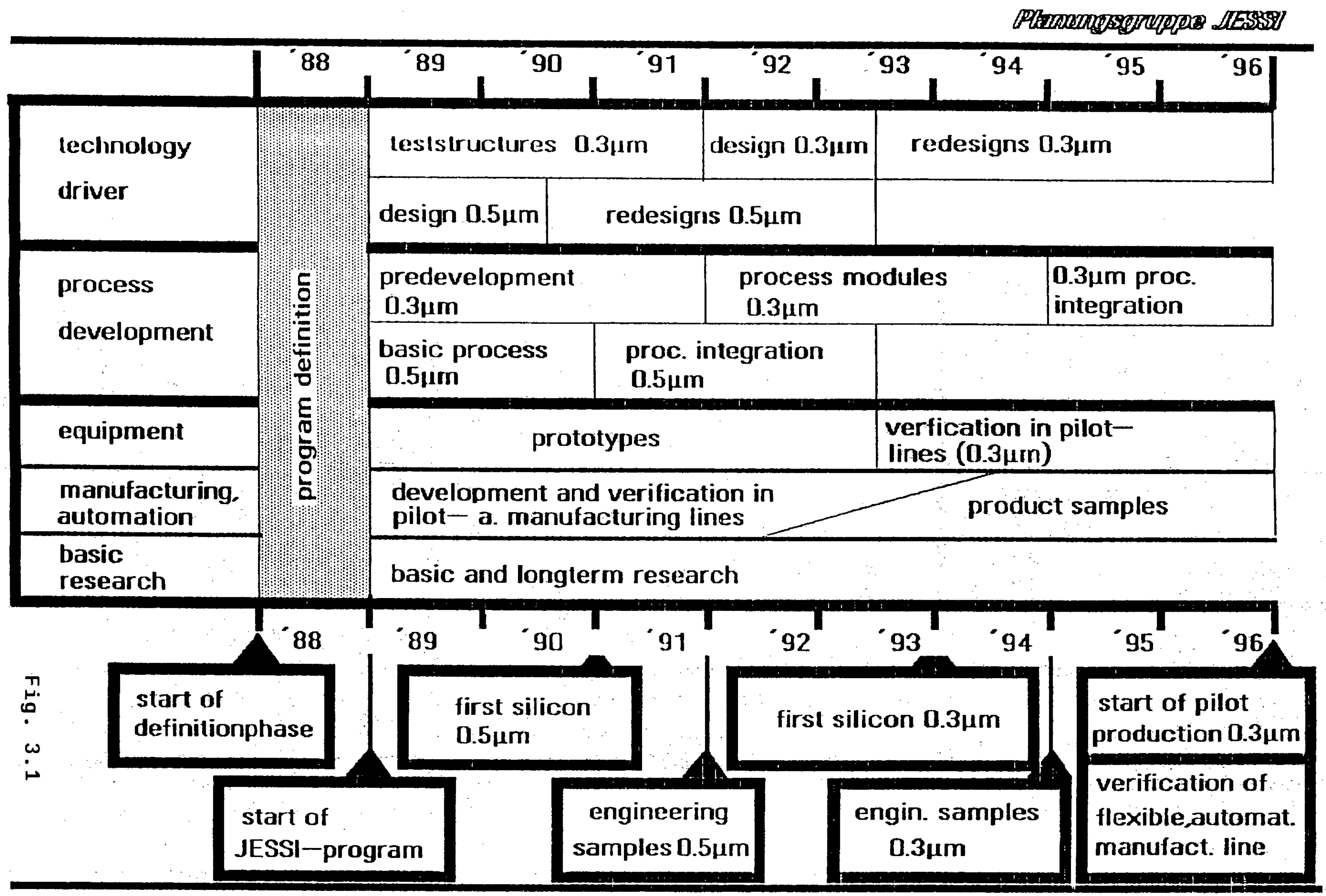

Planungsgruppe JESSI
'88 '89 '90 '91 '92 '93 '94 '95 '96
technology driver
teststructures 0.3µm
design 0.3µm
redesigns 0.3µm
design 0.5µm
redesigns 0.5µm
process development
predevelopment 0.3µm
process modules 0.3µm
0.3µm proc. integration
basic process 0.5µm
proc. integration 0.5µm
equipment
prototypes
verfication in pilot— lines (0.3µm)
manufacturing, automation
development and verification in pilot— a. manufacturing lines
product samples
basic research
basic and longterm research
program definition
start of definitionphase
start of JESSI—program
first silicon 0.5µm
engineering samples 0.5µm
first silicon 0.3µm
engin. samples 0.3µm
start of pilot production 0.3µm
verification of flexible,automat. manufact. line

Fig. 3.1

4. The Role of JESSI Partners

4.1 High Integration Technologies

The leading European IC manufacturers - Philips, SGS-Thomson, and Siemens - are to develop manufacturing technologies for 0.5 and 0.3 μm CMOS technologies, starting from their respective know-how. Tryout of the technological capability has to be achieved by manufacturing of competitive DRAM (VRAM), SRAM, EPROM and logic products. Within JESSI collaboration will concentrate on

- Co-operation in the field of the development of process steps, materials, and equipment with the aim of allowing product exchange and second sourcing.
- Realization of a common equipment strategy as a prerequisite for a viable European equipment industry.
- Co-operation in manufacturing science.
- Common definition of design standards and interfaces in order to allow for the use of a unified European (international) user interface to the IC-makers by the application industry.

A wider co-operation together with other partners on specific technological aspects will be possible.

4.2 Special technologies

Within the subprogram "technology", contributions of semiconductor makers with special process know-how are seen - within the JESSI goals - on e. g. high speed technology, radiation hardness, digital-analog circuitry.

4.3 Manufacturing Engineering

Companies and institutes being involved within the subprogram "equipment and materials" have the task to develop in strategic areas manufacturing equipment, semiconductor materials and to evaluate solutions for mechanisation, automation and clean room techniques (manufacturing science). This has to be achieved on order respectively in agreement with European semiconductor manufacturers.

The following criteria are decisive for the participation in the JESSI Program:

- sufficient technical experience and capability
- new technical concepts
- economically sound European company
- internationally competitive, with corresponding service

Co-operation between equipment manufacturers and the semiconductor industry must be supported by a tight meshing of equipment and process development. However, in the phase of economic exploitation, the equipment manufacturers must not be obstructed on the world market; and the component manufacturer as well must be free to use the best equipment available world-wide for production.

Worldwide co-operation will be necessary, since not all areas will be covered by European supply.

4.4 Application

In the subprogram "application", participants coming from application industries, IC-manufacturers and CA-Design houses are working together. Their tasks are as follows:

- Definition of a CAD base system with standardized interfaces by all major system houses and IC-manufacturers in Europe.
- Realization of the CAD base system using all available ressources.
- Development of additional, application specific CAD-tools by the companies involved in specific Europrojects, integratable into the base system.
- Furthermore the proving of the design environment in advanced Europrojects which have to be defined in important application areas, is a main task in order to demonstrate the capabilities.

4.5 Basic and Longterm Research

Institutes and universities co-operating within the JESSI program have to fulfill the following tasks:

- Longterm research shall develop new methods and processes, (e. g. in the field of technology feature sizes smaller 0,3 μm should be opened up) thereby satisfying the prerequisites for future products.
- Supporting and alternative research will be carried out under industrial orientation.
- The research findings must be made available to industry.

5. JESSI Organization

5.1. Definitions: Program Acception, Proposal Acception and Execution (Fig.5.1)

Three seperated activities have to be distinguished, that partially run in parallel:

(1) Program Definition. Overall Program definition will end at December 31st, 1988 and result in the Greenbook (what to be done, budget estimates) issued in December, 1988 and defining the JESSI outline.

(2) Program Acceptance. Program acceptance will start January 1st, 1989 and will require

- approval by the national govenments , and the CEC, on JESSI program funding for the Greenbook for the years 1989 to 1996 and
- based on the approval of funding a firm committment by the major participating industries towards JESSI

(3) Proposal Acceptance. Proposals will be demanded in a so called Bluebook form, decribing in detail the action to be taken (how to do it) by specific participants (who does it). The responsibilitis are shared:

- industry to label proposals JESSI
  and
- governments to approve funding for proposals

Bluebooks will have different time horizons and will not necessary follow the (sub-) project structure of the Greenbook. The Bluebook(s) will be subject to permanent revision and updating.

The proposal acceptance will start in parallel to program acceptance on Jan. 1st, 1989 will come to an end in 1994.

(4) Execution. Execution of JESSI will cover the period 1989 to 1996.

5.2 Organization of the Execution Phase (Fig 5.2)

JESSI will be highly visible in the world. As such it requires a single, clearly started overall policy. The industrial JESSI Board will reflect JESSI being an

industrial undertaking by having the tasks of

- international representation by the chairman
- external communication of the goals and terms of references
- monitoring of program goals in respect to overall progress, coherence and consistency.

The JESSI-Board will comprise representation of the subprogram Management Boards reflecting the relative importance of the subprograms within JESSI.

The JESSI Board will be supported by a small JESSI Office for clerical work and other management support.

The JESSI Greenbook and (Bluebooks) covering 8 years will be subject to permanent revision and updating, since

- New technologies must flow into the program.
- New research resources emerge.
- New world standards develop.
- Fields of application change it's inportance.
- Industrial groupings may change.
- Governmental and EC policies may change.

Anticipating these changes, JESSI needs to have a flexible organization, processing changes on subprogram level, without destabilizing the JESSI program as a whole. Industrial Management Boards on the subprogram level representing the major participating industries will take care for industrial monitoring and coordination of subprogram progress, coherence, consistency, and adaption.

The representation of the participating industry in the Management Boards will distinct between participants bearing the majority of work (A participants) and others (B participants). The Management Boards nominate their representatives for the JESSI Board. The organization of the Management Boards will vary from subprogram to subprogram.

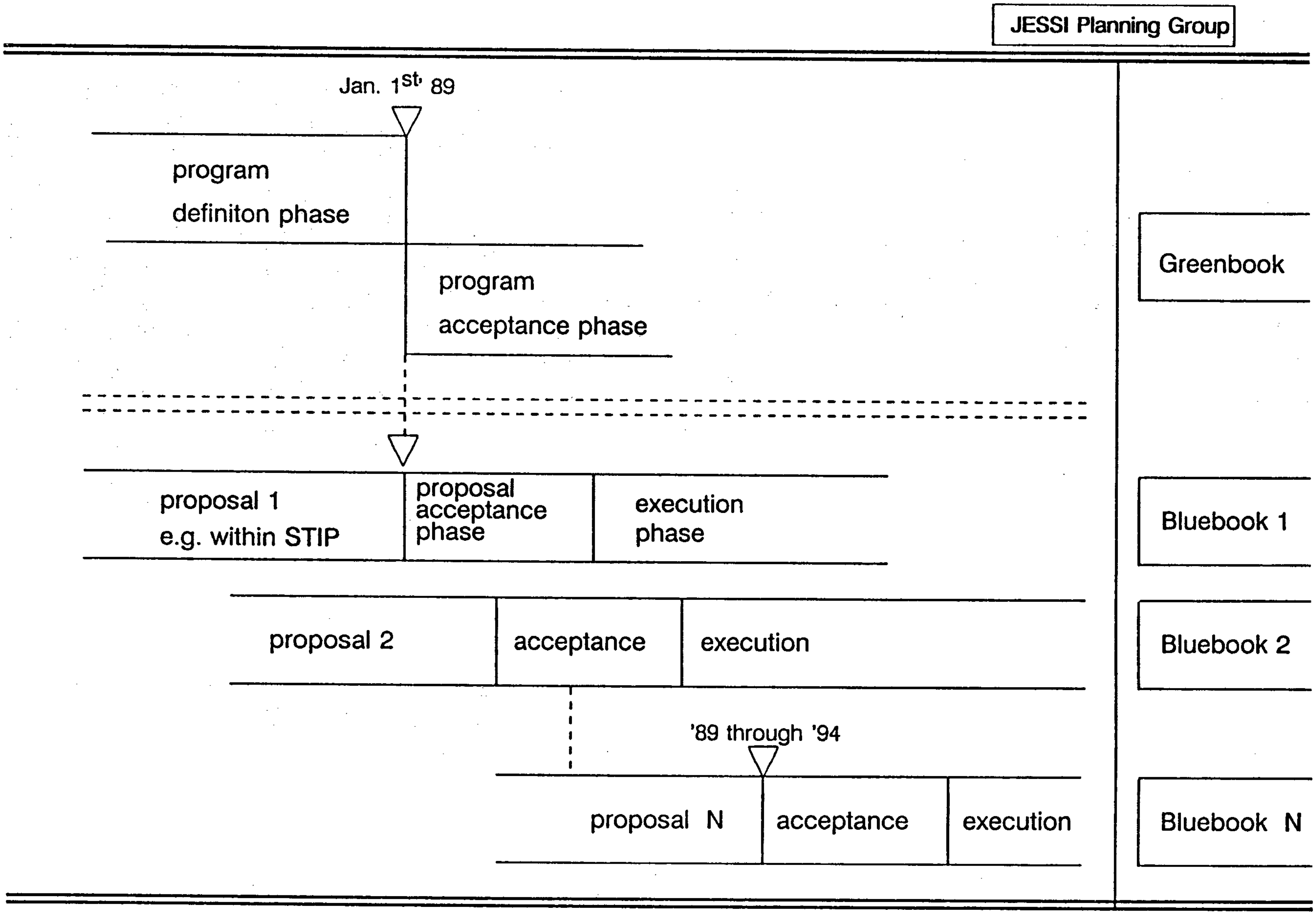
Project managements have to be installed per project under the full responsibility of the participating industry.

A clear cut distinction between responsibilities and tasks of industry and those of

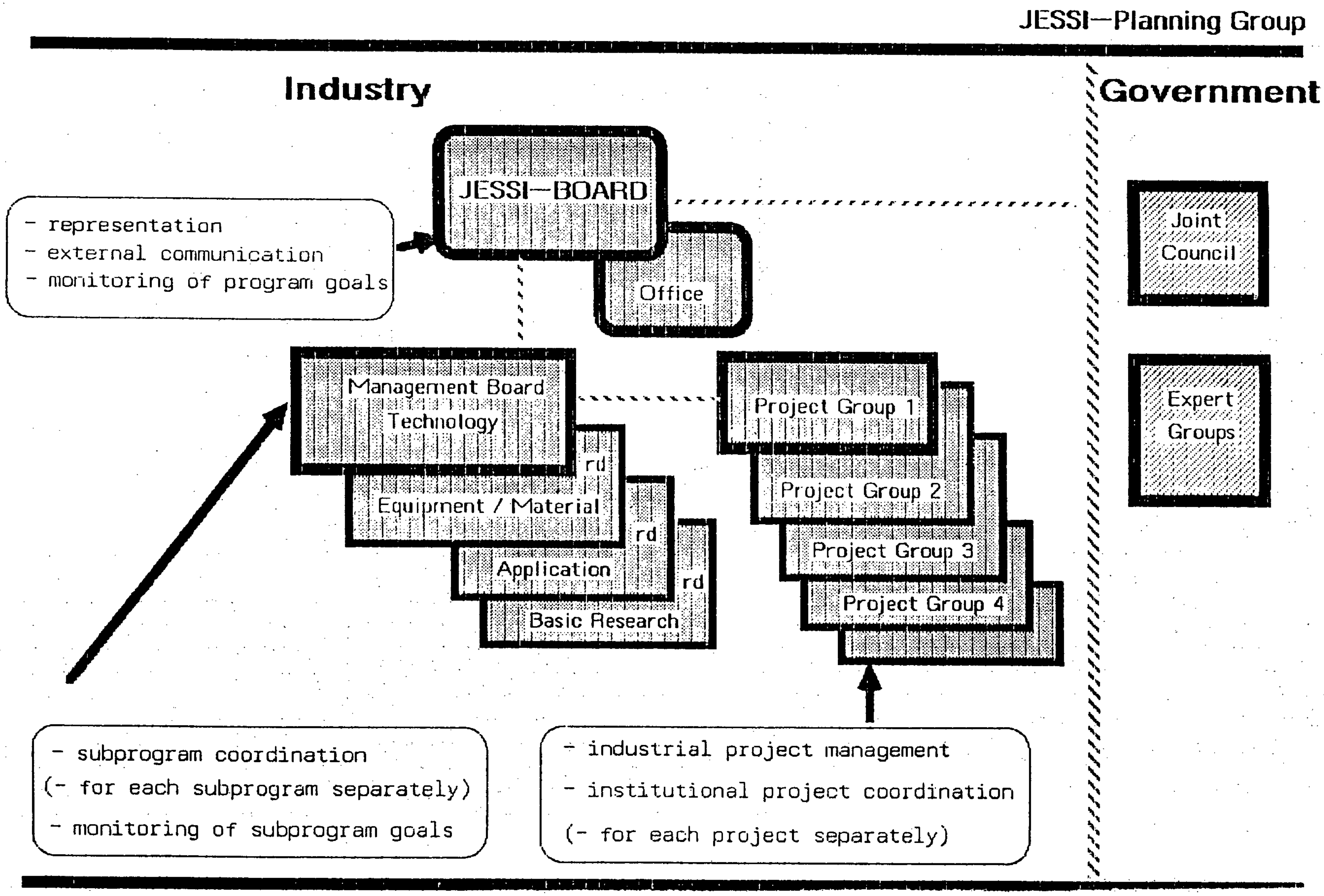
governments/CEC is required. The public sector must formulate the supporting measures and the modalities of applying them. Therefore, a Joint Council of the governments has been proposed for evaluation of the Greenbook and the Bluebooks and to decide on program and proposal acceptance.

It is anticipated, that national Governments and the EC will require independent Expert Groups to support decision making on funding issues. As a general guideline it is proposed:

- to establish one international Expert Groups per subprogram,
- each government (including the EC) participating in the subprogram shall nominate one expert, by preference the same experts for all of the subprograms. Nominees should be well know by industry and science
- on a national level, the national delegate may be backed by national expert teams.



JESSI Planning Group
Jan. 1st, 89
program
definiton phase
program
acceptance phase
proposal 1
e.g. within STIP
proposal
acceptance
phase
execution
phase
proposal 2
acceptance
execution
'89 through '94
proposal N
acceptance
execution
Greenbook
Bluebook 1
Bluebook 2
Bluebook N


JESSI–Planning Group
Industry
Government
- representation
- external communication
- monitoring of program goals
JESSI–BOARD
Office
Joint Council
Expert Groups
Management Board Technology
rd
Equipment / Material
rd
Application
rd
Basic Research
Project Group 1
Project Group 2
Project Group 3
Project Group 4
- subprogram coordination
(- for each subprogram separately)
- monitoring of subprogram goals
- industrial project management
- institutional project coordination
(- for each project separately)

6. Manpower required for JESSI

6.1 Overall JESSI Program

The figures presented below are the total of the four subprograms:

Year	89	90	91	92	93	94	95	96	Σ
Manyear	1685	2615	3090	3145	3120	2940	2615	2190	21400

Distribution per		% of capacity
Subprogram	Technology	29
	Equipment and Materials	15
	Application	34
	Basic and Longterm Research	22

6.2 Technology

Figures for manpower have been calculated independently based on bottom-up planning of experts of the three companies. Considering the strategic targets with respect to cooperation, top down cuttings have been applied resulting in a considerable reduction. It must be stressed that the top-down numbers are only realistic if all possibilities of work- and burden-sharing are exploited.

Project Group	C-MOS-Memories	53
	LOGIC	24
	Manufacturing Engineering	23

6.3 Equipment and Materials

The area of equipment and materials could contain all possible pieces and substances needed in chip manufacturing. This is not necessary. The JESSI planning has estimated priorities in the strategic approach in the scope of need to become not dependent as non European products and of course chances that producers will succeed in reaching objectives.

Project Group	Automation/Clean Room	18
	Lithography-oriented Equipment	17
	Non-Lithography-oriented Equipment	26
	Back-end Processing/Testing	17
	Materials	22

6.4 Application

In view of the late start of the Europrojects and the strong influence of the Europrojects on the product strategies of a large number of European companies, not all projects of the bottom-up planning are consolidated yet.

Further, a merge of some of the Europrojects seems to be desirable, but will only be possible after alignment of the strategies of the participating companies and when definite committments have been made by the companies.

Project Group	Tools and Environment/Support	62
	Europrojects	38

6.5 Basic and Long-term Research

Basic research of roughly 15 - 20 % of the total effort is adapted to needs of applied research and development. In order to cope with contingency, e.g. unforeseen requests in the area of support and alternative research (which is largely on demand by and under guidance of industry) provisions have been made in the estimated manyears. However, priority setting is still necessary for support- and alternative-projects.

Further, duplication between section teams should be avoided in the Bluebooks. The real contribution to the JESSI goals have to be evaluated later, based on the quality of proposers and proposals.

Project Group	Design Methodology	33
	Modelling and Simulation	10
	Advanced Processing Steps	27
	Process Integration	30

7. Cost Structure

7.1 Tariffs

The costs have been calculated using the manpower estimations and applying for each of the subprograms avaraged tariffs (cost per manyear) experienced in other large projects for comparable activities.

For Basic Research it has to be noted, that the avarage tariff considers both, activities within industrial research laboratories as well as public institutes and unversities. In both cases investments are part of the tariff applied.

Costs are based on 1988 ECU. No inflator had been used.

7.2 Overall JESSI Program

Breakdown of Total JESSI Cost per year

Year	89	90	91	92	93	94	95	96	Σ
Cost (MECU)	313	463	543	553	550	520	470	392	3804

Phase 0 — 776 —
Phase 1 — 1096 —
Next Phases — 1932 —

Distribution per Subprogram		% of Cost
	Technology	41
	Equipment and Materials	13
	Application	32
	Basic and Longterm Research	14

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